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(71) Applicant 00003296
DENNKI KAGAKU KOGYO KABUSHIKI KAISHA
1-4-1, Yuraku-cho, Chiyoda-ku
Tokyo, Japan

(72) Inventor Suguru Kawasaki
DENNKI KAGAKU KOGYO KABUSHIKI KAISHA
Omuta Factory
1, Shinkai-cho, Omuta-shi
Fukuoka, Japan

(72) Inventor Mitsuyoshi Iwasa
DENNKI KAGAKU KOGYO KABUSHIKI KAISHA

Omuta Factory
1, Shinkai-cho, Omuta-shi
Fukuoka, Japan

(72) Inventor Masao Tsukijihara
DENNKI KAGAKU KOGYO KABUSHIKI KAISHA
Omuta Factory
1, Shinkai-cho, Omuta-shi
Fukuoka, Japan

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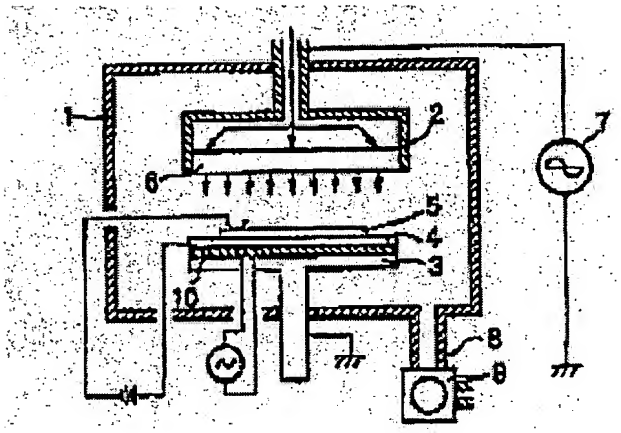
(54) [Title of the Invention]
HIGH-TEMPERATURE INSULATOR

(57) [Abstract]
[Purpose]
A high-temperature insulator having a plasma resistance and an insulating ability at high temperatures suitable for a plasma etching system.
[Constitution]
A high-temperature insulator, wherein substances having a plasma resistance are coated on a molded object of hexagonal boron nitride.
[Effects]
By applying the high-temperature insulator of the present invention to a plasma etching system, the plasma etching of silicon wafers can be attained at high temperatures. Consequently, great contributions are made to manufacturing of semiconductor devices in that reliability of semiconductor devices can be improved by an accelerated etching speed and through finer patterning, and durability of the system can be increased.



1	the vacuum container
2	the top electrode
3	the bottom electrode
4	the chuck
5	the wafer
6	the gas-blowing hole
7	the high-frequency power source
8	the exhaust hole
9	the vacuum pump
10	the heater

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[What Is Claimed Is:]

[Claim 1]

A high-temperature insulator, wherein substances having a plasma resistance are coated on a molded object of hexagonal boron nitride.

[Detailed Description of the Invention]

[0001]

[Industrial Fields of Application]

The present invention relates to a high-temperature insulator having a great plasma resistance used for components such as a plasma etching system.

[0002]

[Prior Art]

Various processes on a microscopic scale such as formation of a pattern are required in making integrated circuits, wherein numerous transistors are formed on a silicon wafer.

[0003]

Etching is a method that is often used for the formation of a pattern. This is a method, wherein a pattern is formed with a resistive material called a resist on a silicon wafer or a conductive or insulating layer formed thereon, and then parts that are not covered with the resist are selectively removed by exposing an etching solution or gas. In general, a method using an etching solution is called wet etching, whereas a method using an etching gas is called dry etching. Furthermore, in dry etching, an etching gas needs to be activated. Activation of an etching gas is performed either by heating a reaction system to a high temperature, e.g., 100℃ or higher, or by deriving reactive gas plasma from an etching gas (plasma etching). For pattern formation, in general, plasma etching is utilized, which can be performed at a relatively low temperature.

[0004]

Recently as the degree of integration of integrated circuits is being improved, much finer patterns are expected be formed. Plasma etching, by which patterns can be formed with a high degree of accuracy, is becoming predominant among others.

[0005]

Among various plasma etching systems, widely used are so-called sheet-fed plasma etching systems, wherein wafers with a large diameter can be directly treated.

[0006]

Figure 1 is a schematic view for illustrating a sheet-fed plasma etching system. In Figure 1, a pair of the top electrode 2 and the bottom electrode 3 is provided in the vacuum container 1 to generate plasma, the wafer 5 being fastened at the chuck 4 of the bottom electrode 3. There are different chucks depending on how to fasten a wafer, such as a mechanical chuck, vacuum chuck, and electrostatic chuck. A wafer needs a margin for fastening to a mechanical chuck, while a vacuum chuck can not be used in vacuum. Therefore, currently, electrostatic chucks are used relatively often. With an electrostatic chuck, electrostatic attraction is generated between the chuck and the wafer by applying a voltage to an electrode inside the chuck for fastening the wafer so that the wafer is secured. Thus, electrostatic chucks can be used in vacuum, and also there is no need to provide the wafer a margin for fastening. Etching gas is provided through the gas-blowing hole 6 of the top electrode 2 into the vacuum container 1. The pair of the top electrode 2 and the bottom electrode 3 are connected to the high-frequency power source 7 to generate plasma discharge, and vacuum is maintained inside the vacuum container by the vacuum pump 9 connected to the exhaust hole 8.

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[0007]

Prior to etching a pattern is formed with a resist, and then air in the vacuum container 1 is exhausted. Next, etching gas is provided to the space between the top electrode 2 and the bottom electrode 3 through the gas-blowing hole 6 of the top electrode 2, and then from this etching gas reactive gas plasma is generated by the high-frequency power source 7. Thus, etching is performed so that parts that are not covered with the resist are reacted with the etching gas. The products of this reaction are removed from the exhaust hole 8.

[0008]

All components of the plasma etching system shown in Figure 1 are exposed to an atmosphere of plasma, hence need to be resistant against plasma, and are made of

substances such as aluminum and alumina. Especially, the surface of the chuck 4 needs to be highly insulating in addition to be plasma resistant, and therefore, in many cases, is coated with alumina. On the other hand, currently, plasma etching is performed while a wafer is heated, so as to increase an etching speed or to form a fine pattern.

[0009]

[Problems to Be Solved by the Invention]

However, in the foregoing method, in other to heat the wafer, it is necessary to heat the chuck 4 as well as the wafer. With the conventional plasma etching system wherein the surface of the chuck is coated with alumina, by heating, in turn, the insulating ability of alumina decreases, causing a dielectric breakdown, and as a result, disadvantageously the wafer cannot be hold at the proper position. For overcoming this disadvantage, hexagonal boron nitride (hBN), which has a greater insulating ability at high temperatures than alumina, is attempted to use for coating. However, because hBN has poor plasma resistance, hBN is etched by plasma and incorporated into the wafer as impurities. As a result, electrical properties of the wafer decrease, which poses another disadvantage.

[0010]

The purpose of the present invention is to overcome the disadvantages arising from the conventional plasma etching system mentioned above to provide a high-temperature insulator having a plasma resistance as well as an insulating ability at high temperatures.

[0011]

[Means for Solving the Problems]

Therefore, the present invention is a high-temperature insulator, wherein substances having a plasma resistance are coated on a molded object of hexagonal boron nitride.

[0012]

Hereafter, further explanation on the present invention is provided. A molded object of hexagonal boron nitride (hBN) is used for the substrate of the high-temperature insulator of the present invention. Molded hBN has a great insulating ability, especially at high temperatures. Examples of molded hBN include sintered objects made of hBN powder by sintering, and molded objects of pyrolytic boron nitride (pBN).

[0013]

On such molded hBN, one or more substances having a plasma resistance are coated to provide the high-temperature insulator of the present invention. A substance having a plasma resistance means a substance that is etched slowly in plasma. An example is a substance whose etching speed is 10 Å/m or less in the high-frequency plasma generated by applying a power of 0.7 kw at 0.1 torr using an equimolar gas mixture of oxygen and tetrafluoromethane (CF_4). Examples of such substances are AlN, SiC, Si_3N_4, etc. as well as aluminum and alumina. Methods such as chemical vapor deposition (CVD), ion plating, and plasma spraying are used for coating such substances.

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[0014]

The high-temperature insulator of the present invention can be of any shape and size. For coating the chuck 4 of the plasma etching system in Figure 1, for example, a substrate, if too thick, hinders heat conduction, resulting in decreased temperature controllability of the wafer, whereas a substrate, if too thin, causes a dielectric breakdown. Therefore, when an electrostatic chuck is made of the high-temperature insulator of the present invention, desirably a substrate has a thickness of 0.01 to 10 mm. On the other hand, a coating of a plasma resistant substance, if too thick, allows delamination to readily occur at the interface with a substrate of molded hBN, whereas a coating of a plasma resistant substance, if too thin, decreases durability, because exposure of the substrate readily occurs. Thus, a coating formed with the substances having a plasma resistance derived from the high-temperature insulator of the present invention desirably has a thickness of 0.001 to 1 mm.

[0015]

A semiconductor wafer is heated by the plasma etching system mentioned above, and then plasma etching is conducted. The heating temperature is 100 to 1000℃, and oxygen, tetrafluorometane (CF_4), tetrachloromethane (CCl_4), etc. are used as an etching gas.

[0016]

Applications of the high-temperature insulator of the present invention should not be limited to an electrostatic chuck of a plasma etching system such as the one mentioned above, but can be extended to semiconductor wafer processes involving heat treatment such as epitaxial growth, CVD, plasma CVD, and physical vapor deposition (PVD).

[0017]

[Examples]

Hereafter, further specific explanation on the present invention is provided with the examples and reference examples.

[0018] Example 1 and Reference Example 1

An high-temperature insulator of the present invention was made, wherein SiC was coated at a thikness of 0.1 mm on one side of a sintered disk of hBN with a thickness

of 1 mm by CVD. Also, an electrode was made by electroless plating of nickel on the other side to obtain an electrostatic chuck.

[0019]

This chuck was mounted to the plasma etching system in Figure 1 via an insulator (not shown), and a tungsten film formed on a silicon wafer was plasma etched. Tetrachloromethane was used as etching gas, a high-frequency power of 200 W was applied between a pair of the top electrode 2 and the bottom electrode 3, also power was supplied to the heater 10 to allow the surface temperature of the wafer to reach to 400℃, and then etching was performed for about 100 seconds. The resulting etching speed was 100 Å/sec.

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[0020]

For comparison, etching was performed in the same conditions as in Example 1 except that the heating step using the heater was not provided. In this case, the surface temperature of the wafer was about 150℃. The resulting etching speed was 20 Å/sec.

[0021] Example 2 and Reference Example 2

A graphite electrode was placed on the top surface of a sintered object of hBN, which then was coated at first with hBN by CVD, and then with AlN to make a high-temperature insulator of the present invention. In this case, respective coating with hBN and with AlN was 0.5 and 0.3 mm thick.

[0022]

This was mounted to the plasma etching system in Figure 1, and a silicon dioxide film formed on a silicon wafer was plasma etched. Tetrafluoromethane was used as etching gas, a high-frequency power of 150 W was applied between the top electrode 2 and the bottom electrode 3, also power was supplied to the heater 10 to allow the surface temperature of the wafer to reach to 300℃, and then etching was performed for about 200 seconds. The resulting etching speed was 150 Å/sec. Furthermore, when semiconductor devices having 4-Mbite memory were made from this wafer, no defective device was found.

[0023]

For comparison, etching was performed in the same conditions as in Example 2

except that the heating step using the heater was not provided. In this case, the surface temperature of the wafer was about 100℃. The resulting etching speed was 60 Å/sec. Furthermore, when semiconductor devices having 4-Mbite memory were made from this wafer, 3 defective devices were found among 100 devices.

[0024] Example 3 and Reference Example 3

The electrostatic chuck made in Example 2 was mounted to the plasma etching system in Figure 1, and a tungsten film formed on a silicon wafer was plasma etched. Tetrachloromethane was used as etching gas, a high-frequency power of 250 W was applied between the top electrode 2 and the bottom electrode 3, also power was supplied to the heater 10 to allow the surface temperature of the wafer to reach to 500℃, and then etching was performed for about 200 seconds.

[0025]

After this etching process was performed on 500 or more silicon wafers, no damage was found on the plasma etching system, and also resulting semiconductor devices showed no decreased electrical properties.

[0026]

For comparison, an electrostatic chuck was made in the same conditions as in Example 3 except that hBN was not coated by CVD, and silicone wafers were etched in the same conditions. The resulting leak current from the electrostatic chuck to the wafer was 100 mA/cm^2 in Reference Example 3, which was greater than that of 0.1 mA/cm^2 in Example 3. As a result, the silicon dioxide film on the silicon wafer was broken, and 90 defective devices were found among 100 semiconductor devices made from this silicon wafer. Moreover, after about 150 silicon wafers were treated, the AlN coating generated a dielectric breakdown.

[0027]

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[Effects of the Invention]

By applying the high-temperature insulator of the present invention to a plasma etching system, the plasma etching of silicon wafers that was conventionally conducted at room temperature can be attained at higher temperatures. Consequently, great contributions are made to manufacturing of semiconductor devices in that reliability of semiconductor devices can be improved by an accelerated etching speed and through finer patterning, and durability of the system can be increased.

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[0028]

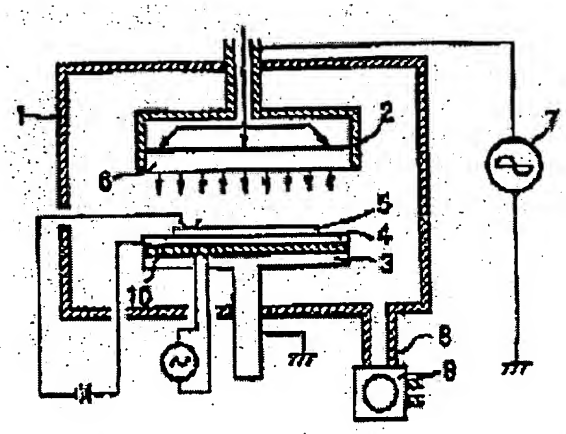
[Brief Description of Drawings]

Figure 1 is a schematic view of the sheet-fed plasma etching system having the high-temperature insulator of the example of the present invention.

[Explanation of Referenced Numerals]

1 ·····the vacuum container
2 ·····the top electrode
3 ·····the bottom electrode
4 ·····the chuck
5 ·····the wafer
6 ·····the gas-blowing hole
7 ·····the high-frequency power source
8 ·····the exhaust hole
9 ·····the vacuum pump
10 ·····the heater

[Figure 1]



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I, Megumi Nozawa, a translator fluent in the Japanese language, on behalf of Morningside Evaluations and Consulting, do solemnly and sincerely declare that the following is, to the best of my knowledge and belief, a true and correct translation of the document(s) listed below in a form that best reflects the intention and meaning of the original text.

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Signature of Translator

Date: November 5, 2005

Description of Documents Translated:

T15800:
3 Japanese Patent Applications, from Japanese to English:
***Kokai* No. H4-238882, *Kokai* No. S64-39728, and *Kokai* No. H3-115535**

450 7th Ave | 6th Floor | New York, NY 10123 | Tel 212.643.8800 | Fax 212.643.0005 | www.msdn.com